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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,547	09/09/2003	Sheng Teng Hsu	SLA 0746	3059
7590	12/28/2004		EXAMINER [REDACTED]	PERKINS, PAMELA E
David C. Ripma Patent Counsel Sharp Laboratories of America, Inc. 5750 NW Pacific Rim Boulevard Camas, WA 98607			ART UNIT [REDACTED]	PAPER NUMBER 2822

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/659,547	HSU ET AL <i>PW</i>	
	<b>Examiner</b>	<b>Art Unit</b>	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 20 October 2004.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-20 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
     1. Certified copies of the priority documents have been received.  
     2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
     3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

This office action is in response to the filing of the request for reconsideration filed on 20 October 2004. Claims 1-20 are pending.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-5, 11 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Gnadinger (6,674,110).

Referring to claims 1 and 5, Gnadinger discloses a method of fabricating a ferroelectric transistor where a semiconductor substrate (20) is prepared; forming a gate stack on the substrate (20), the gate stack comprising a conductive oxide layer (31) overlying and directly contacting the substrate (20); a ferroelectric material layer (30) over the conductive oxide layer (31); and a top electrode conductive layer (50) over the ferroelectric material layer (30); and forming drain and source regions (40 & 41) on opposite sides of the gate stack (col. 5, lines 13-57).

Referring to claims 3 and 11, Gnadinger discloses the electrode conductive layer (30) as a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide (col. 5, lines 44-53).

Referring claims 4 and 12, Gnadinger discloses the conductive oxide layer comprises a conductive perovskite oxide, a high temperature superconducting oxide, or an oxide film of any metal selected from a group consisted of Mo, W, Tc, Re, Ru, Os, Rh, Ir, Pd, Pt, In, Zn, Sn, Nd, Nb, Sm, La, and V (col. 10, lines 51-55).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gnadinger in view of Willer et al. (6,538,273).

Gnadinger discloses the subject matter claimed above except a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer.

Willer et al. disclose a method of fabricating a ferroelectric transistor where a gate stack is formed on a semiconductor substrate (1), the gate stack comprising a conductive layer (4<sub>1</sub>) overlying the substrate (1); forming a bottom electrode conductive layer (4<sub>2</sub>) over the conductive layer (4<sub>1</sub>); forming a ferroelectric material layer (5) over the bottom electrode layer (4<sub>2</sub>); forming a top electrode conductive layer (6) over the

ferroelectric material layer (5); forming drain and source regions (2) on opposite sides of the gate stack; and a dielectric spacer (8) on the sidewall of the gate stack (col. 4, line 63 thru col. 6, line 22). Willer et al. further disclose the formation of the gate stack comprising the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack (Fig.2; col. 5, lines 41-63).

Since Gnadinger and Willer et al. are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Willer et al. would have been recognized in the pertinent art of Gnadinger. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Gnadinger by a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer as taught by Willer et al. to improve punch-through voltage (col. 1, lines 43-64).

Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gnadinger in view of Moon (5,744,374).

Gnadinger discloses the subject matter claimed above except wherein the formation of the gate stack comprised the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack.

Moon discloses a method of fabricating a ferroelectric transistor where a gate stack (20) is formed on a semiconductor substrate (1), the gate stack (20) comprising an oxide layer (11) overlying the substrate (1); forming a ferroelectric material layer (12) over the oxide layer (11); forming a top electrode conductive layer (13) over the

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ferroelectric material layer (12); forming drain and source regions (9) on opposite sides of the gate stack (20).

Referring to claim 7, Moon further discloses the formation of the gate stack (20) comprising the deposition of the multilayer gate stack (20), the photolithography patterning (16) of the gate stack (20) and the etching of the gate stack (20) (col. 4, line 58 thru col. 5, line 33).

Referring to claim 8, Moon discloses wherein the formation of the drain and source regions (9) comprises an implantation to form a high doping concentration into the source and drain regions (9) (col.6, lines 25-34).

Referring to claim 9, Moon discloses wherein the formation of the drain and source regions (9) comprises an implantation to form a LDD ion implantation into the source and drain regions (9) (col.6, lines 25-34).

Referring to claim 10, Moon discloses a dielectric spacer (18) on the sidewall of the gate stack (20) (col. 6, lines 1-34).

Since Gnadinger and Moon are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Moon would have been recognized in the pertinent art of Gnadinger. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gnadinger by the formation of the gate stack comprised the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack as taught by Moon to decrease operation voltage (col. 2, lines 1-20).

Claims 13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gnadinger in view of Sakai et al. (2003/0067022).

Gnadinger disclose the subject matter claimed above except forming a replacement gate stack on the substrate, the replacement gate stack which includes a sacrificial layer; forming drain and source regions on opposite sides of the replacement gate stack; filling the area surrounding the replacement gate stack while exposing the top portion of the replacement gate stack; removing the sacrificial layer portion of the replacement gate stack; forming the remainder of the gate stack.

Sakai et al. disclose a method of fabricating a ferroelectric transistor where a replacement gate stack is formed on a semiconductor substrate (1), the replacement gate stack comprising an oxide layer (40,3) overlying the substrate (1); and a sacrificial layer (42) over the oxide layer (40,3) (Fig. 4A); forming drain and source regions (7,8) on opposite sides of the replacement gate stack (Fig. 4B); filling the areas surrounding the replacement gate stack while exposing the top portion of the replacement gate stack; removing the sacrificial layer (42) portion of the replacement gate stack (Fig. 4E); forming the remainder of the gate stack, the remainder of the gate stack comprising a ferroelectric material layer (45) and a top electrode conductive layer (46) (para. 94-100).

Since Gnadinger and Sakai et al. are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Sakai et al. would have been recognized in the pertinent art of Gnadinger. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gnadinger by forming a replacement gate stack on the substrate, the

replacement gate stack which includes a sacrificial layer; forming drain and source regions on opposite sides of the replacement gate stack; filling the area surrounding the replacement gate stack while exposing the top portion of the replacement gate stack; removing the sacrificial layer portion of the replacement gate stack; forming the remainder of the gate stack as taught by Sakai et al. to increase density and reduce cell area (para. 15).

Referring to claim 15, Sakai et al. disclose the sacrificial layer (42) comprising silicon nitride or silicon dioxide (para. 94, 99).

Referring to claim 16, Sakai et al. disclose depositing of a dielectric film (43); and the planarization of the deposited dielectric film (43) to expose the top portion of the replacement gate stack (Fig. 4C; 4D).

Referring to claim 17, Sakai et al. disclose forming the remainder of the gate stack by depositing the ferroelectric material layer (45), the planarization of the ferroelectric material layer (45), the deposition of the top electrode conductive layer (46); the photolithography patterning of the top electrode conductive layer (46), and the etching of the top electrode conductive layer (46) (para. 94-100).

Referring to claim 18, Sakai et al. disclose the formation of the replacement gate stack comprises the deposition of the replacement gate stack, the photolithography patterning of the replacement gate stack and the etching of the replacement gate stack (para. 94).

Referring to claim 19, Gnadinger discloses the electrode conductive layer as a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide (col. 5, lines 44-53).

Referring claim 20, Gnadinger discloses the conductive oxide layer comprises a conductive perovskite oxide, a high temperature superconducting oxide, or an oxide film of any metal selected from a group consisted of Mo, W, Tc, Re, Ru, Os, Rh, Ir, Pd, Pt, In, Zn, Sn, Nd, Nb, Sm, La, and V (col. 10, lines 51-55).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gnadinger in view of Sakai et al. as applied to claim 13 above, and further in view of Willer et al.

Gnadinger discloses the subject matter claimed above except a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer.

Willer et al. disclose a method of fabricating a ferroelectric transistor where a gate stack is formed on a semiconductor substrate (1), the gate stack comprising a conductive layer (4<sub>1</sub>) overlying the substrate (1); forming a bottom electrode conductive layer (4<sub>2</sub>) over the conductive layer (4<sub>1</sub>); forming a ferroelectric material layer (5) over the bottom electrode layer (4<sub>2</sub>); forming a top electrode conductive layer (6) over the ferroelectric material layer (5); forming drain and source regions (2) on opposite sides of the gate stack; and a dielectric spacer (8) on the sidewall of the gate stack (col. 4, line 63 thru col. 6, line 22). Willer et al. further disclose the formation of the gate stack

comprising the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack (Fig.2; col. 5, lines 41-63).

Since Gnadinger and Willer et al. are both from the same field of endeavor, a method of fabricating a ferroelectric transistor, the purpose disclosed by Willer et al. would have been recognized in the pertinent art of Gnadinger. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Gnadinger by a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer as taught by Willer et al. to improve punch-through voltage (col. 1, lines 43-64).

### ***Response to Arguments***

Applicant's arguments filed 20 October 2004 have been fully considered but they are not persuasive. As stated above, Gnadinger in view of Sakai et al. disclose the method of fabricating a ferroelectric transistor as described in claims 1, 5 and 13.

In response to the applicant's arguments, the applicant argues prior art does not teach forming a conductive oxide layer overlying and directly contacting the substrate. However, Gnadinger discloses forming a conductive oxide layer overlying and directly contacting the substrate.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571)

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272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP



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